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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/401,765	09/23/1999	PHILIP J. CALAMATAS	WAB98553	5126

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EXAMINER
GOSSAGE, GLENN A

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 10/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

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	9

DATE MAILED:

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☑ This application has been examined ☑ Responsive to communication filed on 8-12-02 and 9-11-02 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), ~~_____~~ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____.

Part II SUMMARY OF ACTION

1. ☑ Claims 4-10 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☑ Claims 1-3 have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☑ Claims 4-10 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☑ The proposed additional or substitute sheet(s) of drawings, filed on 9-11-02 has (have) been ☐ approved by the examiner; ☑ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev. 2/93)

☆ U.S. GOVERNMENT PRINTING OFFICE: 1995-391-982

1. The request filed on August 12, 2002 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/401,765 is acceptable and a CPA has been established. An action on the CPA follows.

2. At the outset, it is noted that the amendment filed September 11, 2002 does not appear to be entirely proper since a "clean" copy of the amendments to the specification was not provided as required by 37 CFR 1.121. [While the remarks on page 1 of the amendment indicate that a "clean form" version of all paragraphs was presented, both sets of amendments appear to be marked-up versions.] Applicant should provide a "clean" version of the amendments to pages 1-2 and 6-7 in accordance with 37 CFR 1.121 to avoid possible issue review or printing errors, should any patent issue based on this application.

3. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on September 11, 2002 have been disapproved by the Examiner.

The drawings are objected to because in Figure 1B (as amended), the addition of the "boxes" labeled "DSP" and "CPLD" while deleting the labels "(DSP CHIP)" and "(OTHER CHIPS)" does not appear to be clearly supported by the disclosure as originally filed and may constitute NEW MATTER. [Should the added "boxes" labeled DSP and CPLD be placed within their respective "boxes," adjacent to the labels "(DSP CHIP)" and "(OTHER CHIPS)?"]

Clarification by way of amendment and/or explanation is required.

Additionally, many of the drawings added in the response filed September 11, 2002 do not appear to be necessary to illustrate the invention as claimed and would appear to cloud or obfuscate the invention. It appears only those Figures necessary for a complete understanding of the invention, i.e. necessary to adequately and accurately illustrate and describe the invention, should be retained.

The remaining drawing changes submitted in the response filed September 11, 2002 are acceptable but should be resubmitted for proper approval and entry by the Examiner.

It is also noted here that new Figures 3A-14 added in the amendment filed September 11, 2002 have not been checked by the Examiner to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in these Figures. In this regard, also note the objection to the specification below.

Applicant is again REQUIRED to submit a proposed drawing correction in response to this Office action. However, actual formal correction of the noted defect(s) can be deferred until the application is allowed by the examiner.

Also note MPEP 608.02(r) and (v).

The drawings are also objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "additionally included" self-locking data bus circuits of claim 6, and the complex programmable logic device of claims 6, 8 and 9, must be shown or the features canceled from the claims. No new matter should be entered.

4. It is once again noted here that the specification, particularly the lengthy material (approximately 35 pages) added at the end of the specification, has not been checked by the Examiner to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the disclosure. The following objections are specifically noted:

In the specification:

The specification is objected to as not being sufficiently concise as required by 35 U.S.C. 112, first paragraph, and 37 CFR 1.71, i.e. the description contained in the specification is not as short and specific as is necessary to describe the invention adequately and accurately. See MPEP 608.01(a) and 37 CFR 1.71, as well as the legislative history thereof. Here, the majority of the material added in the amendment filed September 11, 2002 does not appear to be necessary to describe the claimed invention adequately and accurately, and appears to obfuscate or cloud the invention. The specification should be amended or redacted so that only those

portions necessary to adequately and accurately describe the claimed invention are retained.

Again note that these are merely exemplary. The entire specification should be carefully and completely reviewed to ensure that all possible errors are located and corrected.

Appropriate correction is required.

5. It is again noted here that this application appears to contain claims directed to distinct inventions.

More specifically, claim 4 sets forth a "self-locking memory circuit" for a tri-state data bus, which appears to be a subcombination of the "programmable system" of claims 5 and 8, which programmable system includes "self-locking data bus circuits." However, combination claims 5 and 8 not setting forth the details of the subcombination claim appear to provide evidence that the combination as claimed does not require the particulars of the subcombination for patentability. Additionally, the subcombination appears to have separate utility such as a self-locking memory circuit for different circuits in a computer or data processing system (in this regard, also see page 2, lines 1-5 and page 6, lines 2-5 of the originally filed specification). Since the inventions have been shown to be distinct for the reasons outlined above, a requirement for restriction would appear to be in order. [In this regard, also see MPEP 806.05(c).]

Again, while these inventions appear to be distinct, a restriction requirement is NOT being

made at this time since it does not appear there will be a substantial burden on the Office if restriction is not required, given that there are a limited number of claims in each group and since the searches for the different groups overlap to some extent.

However, restriction may be required in the future depending on how the claims are amended. In this regard, attention is again respectfully directed to MPEP 811.

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 10 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification as originally filed does not appear to provide an adequate written description of, or otherwise provide support for, a ratio between the resistance (of the resistor in the self-locking data bus circuit) and the output impedance of the non-clocked, non-inverting amplifier chip being "approximately 4 to 1" as now claimed.

7. Claims 4-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for

failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 4, as well as claims 5 and 8 and therefore their respective dependent claims, it is not entirely clear what is meant by an "electrically noisy" environment here, since whether a circuit is considered to be "noisy" is relative (a circuit which outputs the same amount of electrical noise may be considered in one environment to be "noisy" while in another environment may be considered to be relatively "quiet" or not "noisy"), and since there does not appear to a definition or other guidance what is meant by "electrically noisy" in this context. Thus, one of ordinary skill in the art would not be fairly apprised of the scope of the claim. In this regard, also see MPEP 2173.05(b).

In claim 6, the language "system additionally includes self-locking data bus circuits" is confusing and not entirely clear here, as it is not readily apparent how the additionally included self-locking data bus circuits of claim 6 are connected or related, if at all, to the self-locking data bus circuits of claim 5 (note Figures 1A-1B, e.g.).

In claim 7, it is not entirely clear how "each of said self-locking data bus circuits ... causes respective ones of said self-locking data bus circuits to change state." It appears "(said) respective ones of said" in lines 8 and 10 should be changed to --that--, and "circuit" in lines 9 and 11 changed to --circuit-- for clarity. See also claim 9, lines 8-11 which should be similarly amended for clarity and consistency.

In claim 10, lines 2 and 3, the proper antecedents for "said resistance" and "said self-locking

data bus circuits" is not clear. [Should the claim depend from claim 9 instead of claim 8 and language such as -- , in each of said self-locking data bus circuits, -- or other similar language be inserted after "wherein" in line 2 for clarity? Note that there are plural self-locking data bus circuits set forth in claim 9, each with a resistor having a predetermined electrical resistance and a non-clocked, non-inverting amplifier chip.]

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

Claim 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Buch.

With respect to claim 4, Buch discloses a "self locking" memory or bus latching circuit for a tri-state data bus having multiple bit or data lines, the memory or latching circuit including a non-inverting buffer or amplifier (note 64, 66 together, e.g., in Figure 5, as well as column 5, lines 58-62) for connection to one of the bit or data lines, and a resistor (68 in Fig. 5, e.g.) having a predetermined electrical resistance connected across the buffer or amplifier. [Again note that while two inverters are shown in Figure 5, Buch also teaches that a non-inverting amplifier may

be used in place of the pair of inverters 64, 66 (see column 5, lines 60-62, e.g.)]

The memory or bus latching circuit maintains or stores the level of data on the bus until a subsequent data or voltage level is driven onto the data bus. The resistance value may be chosen to adjust the thresholds at which the circuit will change state. In this manner, the memory or latching circuit has upper and lower "threshold" voltage thresholds that cause the buffer chip or latching circuit to change states when a level of voltage applied to the chip and the resistor "passes through" one of the thresholds. The memory or latching circuit is "self-locking" and does not change state until a voltage is again applied to the data bus which "passes through" one of the thresholds. See column 5, lines 31-35; column 5, line 56 to column 6, line 2; column 6, line 61b to column 7, line 5; and Figure 5, for example.

In this regard, applicant's arguments filed September 11, 2002 have been considered but are not persuasive.

The argument that the invention as claimed is for use "In an electrically noisy environment" (response at page 48) is not persuasive because statements of intended use have no patentable weight in claims drawn to structure. That is, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963), as well as MPEP 2111.02. Note also that the term "electrically noisy" is somewhat vague as discussed above, and

what constitutes an electrically noisy environment is relative. Moreover, since the bus holding circuit of Buch maintains or holds the bus at a stable level in the presence of small electrical signals (below the threshold amount, e.g.), the bus holding circuit may be considered to be used in an "electrically noisy" environment.

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buch.

With respect to claims 5 and 7, Buch discloses a "programmable" computer system including a tri-state data bus electrically connected to a central processing unit (CPU), and a plurality of "self-locking" data bus latching or memory circuits connected to respective bit or data lines of the data bus. Buch teaches that the "self locking" data bus latching circuit may include a non-inverting buffer or amplifier and a resistor having a predetermined electrical resistance connected across the buffer or amplifier (see numbered paragraph 7 above, e.g.), so that the data bus latching circuit maintains or stores the level of data on the bus until a subsequent data or voltage level of a sufficient amount is driven onto the data bus. In this way, different components of the computer system operating at different rates may communicate over the data bus, while

maintaining data integrity and allowing faster bus switching times.

Buch teaches that the bus may be a communication link between one or more computer components, and that the various components of the computer system may be "nodes" comprised of large scale integrated circuits or chips (see column 1, lines 14-39, e.g.), but does not specifically teach that the large scale integrated circuits or chips or components of the system are comprised of a CPU and a "digital signal processor" (DSP) having different rates at which they operate in performing their respective functions.

However, Bush does teach that the components may comprise any typical components used commonly with data buses (see column 3, line 56 to column 4, line 5, e.g.), and it would have been readily obvious to a person of ordinary skill in the art at the time the claimed invention was made to utilize large scale integrated circuit components or chips such as digital signal processors, which are commonly used with data buses, as the large scale integrated circuits in Buch, so that the data bus latching or memory circuits may be used to maintain or store values on the data bus and allow appropriate communication between the different chips.. It would have been obvious to use such data bus latching circuits because Buch teaches that delays due to "hand off" or transitions on the tri-state data bus may be avoided, thereby increasing bus utilization and data bandwidth, while also maintaining the integrity of the data on the bus to allow sampling by the different components, highly desirable features in a computer or communication system (note column 1, line 55 to column 2, line 64, e.g.).

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buch as applied to claims 5 and 7 above, and further in view of Chiang et al.

With respect to claims 6, 8 and 9, Buch discloses a "programmable" computer system including a tri-state data bus electrically connected to a central processing unit (CPU), and a plurality of "self-locking" data bus latching or memory circuits connected to respective bit or data lines of the data bus. Buch teaches that the "self locking" data bus latching circuit may include a non-inverting buffer or amplifier and a resistor having a predetermined electrical resistance connected across the buffer or amplifier (see numbered paragraph 8 above, e.g.), so that the data bus latching circuit maintains or stores the level of data on the bus until a subsequent data or voltage level of a sufficient level is driven onto the data bus. In this manner, different components of the computer system operating at different rates may communicate over the data bus, while maintaining data integrity and allowing faster bus switching times.

Buch teaches that the bus may be a communication link between one or more computer components, and that the various components of the computer system may be "nodes" comprised of large scale integrated circuits or chips including a CPU (see column 1, lines 14-39, e.g.), but

does not specifically teach that the large scale integrated circuits or chips or components to which the bus hold circuit is connected include a complex programmable logic device (PLD). However, as noted above, Bush does teach that the components may comprise any typical components used commonly with data buses.

Chiang et al similarly discloses a bus hold circuit including a resistance and a non-inverting amplifier, and similarly teaches that the bus hold circuit may be used with busses coupled to integrated circuits and specifically teaches that the bus hold circuit may be used with complex programmable logic devices (CPLDs) to hold or latch the data on the bus (see column 1, lines 13-54 and Figure 1, e.g.).

It would have been readily obvious to a person of ordinary skill in the art at the time the claimed invention was made to utilize large scale integrated circuit components or chips such as complex programmable logic devices, as taught by Chiang et al, which CPLDs are commonly used with data buses, in conjunction with the self-locking circuits of Buch, so that the data bus latching or memory circuits may be used to maintain or store values on the data bus and allow appropriate communication between the different chips, including CPUs and CPLDs. It would have been obvious to use such data bus latching circuits because Buch and Chiang et al teach that the states on the data bus may be reliably held between "drives" or when the bus is not being driven but can be overwritten or overcome by the drivers to obtain a new state, and because Buch teaches that delays due to "hand off" or transitions on the tri-state data bus may be avoided, thereby increasing bus utilization and data bandwidth, while also maintaining the integrity of the

data on the bus to allow sampling by the different components, highly desirable features in a computer or communication system (note column 1, line 55 to column 2, line 64 of Buch, e.g.), particularly one using chips such as CPUs, DSPs and CPLDs.

In short, the combined teachings of the references renders obvious a structure on which applicant's claims read, and thus the invention as set forth in the claims would have been obvious, within the meaning of 35 U.S.C. 103, in light of the combined teachings of the references.

With respect to claim 10, insofar as definite and clear, Buch teaches that the resistance values in the bus hold circuit may be adjusted depending on the user's design requirements and may fall anywhere between a maximum determined by the need to maintain valid logic states on the bus and the DC loading of the bus, and a minimum value just sufficiently high that the drivers can overcome the latch (see column 6, line 68 to column 7, line 5, e.g.). Chiang et al similarly teaches that the resistance may be chosen so as to enable an input signal to change the state on the bus (see column 5, lines 40-44, e.g.). Since the bus holding circuits of Buch and Chiang et al maintain or hold the busses at a stable level in the presence of electrical signals (below a threshold amount, e.g.), the bus holding circuits may be considered to be used in an "electrically noisy" environment. While Buch and Chiang et al do not specifically teach adjusting the resistance values to obtain a ratio of "approximately" 4 to 1, the adjustment of the resistance value in Buch and Chiang et al through routine experimentation to operate the bus hold circuit in

an "electrically noisy" environment and obtain a ratio of 4 to 1 would have been readily obvious to one of ordinary skill in the art at the time the claimed invention was made and, as such, does not patentably define the claimed invention over the prior art.

11. Applicant's arguments filed September 11, 2002 have been considered but are not persuasive. It is believed applicant's arguments have been addressed in the preceding paragraphs.

Also, with respect to claims 5-10, the argument that Buch does not specifically teach the interconnection of a CPU with either or both of a DSP and a CPLD through the tri-state data bus having self-locking data bus circuits (response at pages 49-50) is not persuasive because, as discussed above, Buch teaches that the bus may be a communication link between one or more computer components, and that the various components of the computer system may comprise any typical components used commonly with data buses (see column 3, line 56 to column 4, line 5, e.g., as well as column 1, lines 14-39).

One of ordinary skill in the art at the time the claimed invention was made would have found it readily obvious to utilize "typical" components such as a digital signal processor (which is merely a processor which processes digital signals) and a ("complex") programmable logic device, both of which are large scale integrated circuit components or chips commonly used with data buses, particularly in light of the specific teachings of Chiang et al. It would have been obvious to use the self-locking data bus circuits on such typical components because Buch teaches that the data bus latching or memory circuits may be used to maintain or store values on

the data bus and allow appropriate communication between the different chips, and because Buch teaches that delays due to "hand off" or transitions on the tri-state data bus may be avoided, thereby increasing bus utilization and data bandwidth, while also maintaining the integrity of the data on the bus to allow sampling by the different components, highly desirable features in a computer or communication system (again note column 1, line 55 to column 2, line 64, e.g.).

A requirement that Buch specifically mention a DSP as the typical component to be used is tantamount to requiring a reference to expressly teach or anticipate the claimed invention under 35 U.S.C. 102. Here, the reduction or avoidance of delays due to transitions in a tri-state bus and accompanying improvement in data bandwidth and integrity, coupled with the teaching of using the self-locking data bus circuit in conjunction with typical computer components and large scale integrated circuits commonly used with data buses, as specifically taught by Buch, provide ample motivation and suggestion to utilize the self-locking data bus circuits of Buch in conjunction with computer components commonly used with data buses such as DSPs and CPLDs. The proposed modification is not "arrived at (only) through applicant's own disclosure" as contended by applicant (response at page 50) but is based on the teachings and motivation provided by the reference.

Again, since the claims "read on" a structure rendered obvious by the teachings of the reference, the invention as set forth in the claims would have been obvious, within the meaning of 35 U.S.C. 103.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Warner is again noted of interest as discussing adjusting the value of the resistance in a bus hold circuit depending on the user's requirements, including selecting a value for the resistance to reliably hold down the bus line while allowing sufficiently fast transitions on the bus.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn Gossage whose telephone number is (703) 305-3820.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Yoo, can be reached on (703) 308-4908.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)
(703) 746-7239 (Official Communications)

(703) 746-5713 (Use this FAX number only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal paper/amendment be faxed directly to him or her on occasion.)

GLENN GOSSAGE
PRIMARY EXAMINER
ART UNIT 2187